Amendments to the Specification

On page 7, lines 15-30, please amend as shown.

The invention will now be explained in more detail, with reference to the accompanying drawings, in which:

Fig. 1 shows ~~a diagrammatical~~ in cross-section a first embodiment of the trench isolation structure according to the invention;

Fig. 2 shows ~~a diagrammatical~~ in cross-section a second embodiment of the trench isolation structure according to the invention;

Figs. 3a-g show a block diagram of ~~a first~~ the first embodiment of the method according to the invention, resulting in the trench isolation structure of Fig. 1;

Figs. 4a-e show a block diagram of ~~a second~~ the second embodiment of the method according to the invention, resulting in the trench isolation structure of Fig. 2; and

Fig. 5 shows a diagrammatic cross-section of a semiconductor device isolated by means of trench isolation structures according to the invention.

Fig. 6 shows a diagrammatic[[a]] third embodiment of the trench isolation structure according to the invention.

On page 8, lines 1-9, please make changes as shown.

A trench groove is indicated by 4. The trench groove 4 comprises ~~an liner 5 of~~ a liner 5 of a first insulating material, a first filler material 6, a second insulating material 7, having an upper surface 7a and a lower surface 7b and a second filler material 8.

A shallow trench is indicated by reference numeral 9.

The semiconductor slab 1 is made of silicon, or another suitable semiconducting material, and serves as a substrate for e.g. semiconductor devices. Here, the slab of semiconducting material is a lightly doped p material (p-), although n materials are not excluded. As shown in Fig. 1, the trench structure, according to an embodiment of the present invention, is depicted in three parts, a 1st part, 2nd part, and a 3rd part, so as to aid in the discussion herein.

On page 8, after lines 16-19, please insert the following additional text.

It should be noted that, for the purposes of this invention, the assembly of semiconductor slab 1, buried layer 2 and epitaxial layer 3 is sometimes also called the semiconductor slab. The context will indicate clearly the cases whether the assembly is meant, or whether specifically the semiconductor slab, or substrate, is meant.

The dimensions of the features may be described in reference to Fig. 1, a cross-section of the structure according to an embodiment of the present invention. For the purposes of discussion, a "thickness" of a feature is measured in a horizontal direction parallel to the surface of the semiconductor slab, as denoted in the Fig. 1. A "depth" of a feature would be a measured in a direction perpendicular to the surface of the semiconductor slab, also denoted in Fig. 1. The "length" of a feature is measured in a direction perpendicular to the cross-section, denoted in Fig. 1.